IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Applicants: | Brenton A. Baugh, Tanya J. Snyder, and Kendra Gallup | | |
| Assignee: | Agilent Technologies, Inc. | | |
| Title: | Optoelectronic Device Packaging With Hermetically Sealed Cavity And Integrated Optical Element | | |
| Serial No.: | 10/666,091 | Filing Date: | September 19, 2003 |
| Examiner: | Sheila V. Clark | Group Art Unit: | 2815 |
| Docket No.: | 10030386-1 | | |

San Jose, California

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

**DECLARATION OF PRIOR INVENTION PURSUANT TO 37 C.F.R. § 1.131**

I, Brenton A. Baugh, hereby declare that:

1. I conceived of an invention covered in U.S. Patent Application No. 10/666,091 before October 30, 2002, while working in San Jose, CA, U.S.A.;

2. Accompanying this declaration as Exhibit A are copies of notebook pages that were handwritten by me in San Jose, CA, U.S.A., before October 30, 2002;

3. The drawings on the notebook pages illustrate packaging for side-emitting laser diode chips in which output beams from the laser diode chips reflect from respective surfaces of caps that respectively enclose the laser diode chips;

3. Dates on the copies of the notebook pages, which indicated the dates of the original writing, have been redacted but the redacted dates are all before October 30, 2002;

4. An embodiment of the invention was reduced to practice on or before April 8, 2003 by construction of a proto-type device; and

5. From a date prior to October 30, 2002 to the reduction to practice described above, I and the other co-inventors named on the above-identified patent application worked with due diligence to achieve the reduction to practice.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that

THE PATENT LAW OFFICES
OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

PH: (408) 927-6700
FX: (408) 927-6701

these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Brenton A. Baugh — 12/21/04

Brenton A. Baugh — Date

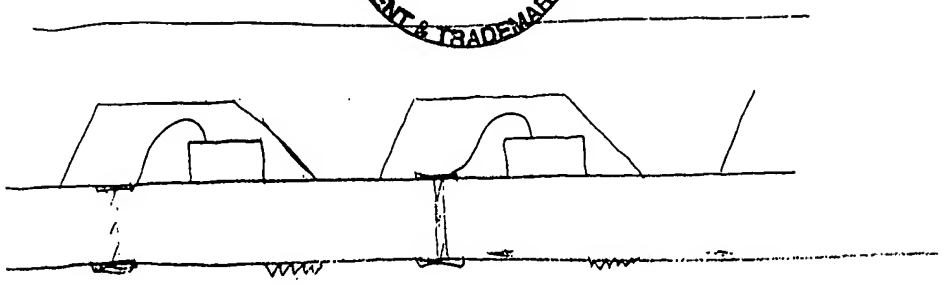
THE PATENT LAW OFFICES
OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

PH: (408) 927-6700
FX: (408) 927-6701

EXHIBIT A

Low Cost Possibility





[redacted]

[redacted]

IC's - Mike Robinsonis

Wafer Costs - 8 inch process

$~~4600~~ 4900 for volumes less than 41 wafers per 6 months

$0.1738 / mm²

Ferrites cost $0.80 per piece

Typical Sizes

Tx- Wires 1.62 x 2.64
Rx- Stacks 1.62 x 1.62

Wafer Test - approaches cost of die

~~0.08~~ $0.008 per second / per Die →

10 seconds

~85% yield at test

90% yield at Die Prep

$3 for microcontroller (Optical mouse $0.08)

Wang Liang - Duracell, Frederick Cheng - Custom Microcontroller

[redacted]

Knightsbridge

## 4L LENSES

Polysilicon 600 Å
Oxide Stop 50 Å
} PECVD Plasma Enhanced

Thickness within 5% Cost - 2-3% Typical
Index Control 2-3%

## B.Bi

$50 for a pair @ 100 MEG/bit

---

Interoperate @ SFF & SFP
Focus on Sonet & Ethernet
155 - 2G4/s